Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-33 (canceled)

Claim 34 (original): A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more transistors with active areas therebetween;

creating an insulating layer overlying the transistors and active areas;

forming a hard mask over the insulating layer;

patterning the hard mask to define cell contacts above the active areas and buried bit lines between the cell contacts;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing spacers to substantially fill the buried bit line trenches;

removing portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts;

recess the spacers within the buried bit lines; and

deposit conductive material within the buried bit line trenches and the cell contact trenches.

Claim 35 (original): A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more FET transistors with active areas therebetween;

creating an insulating layer overlying the transistors and active areas;

patterning the insulating layer to define cell contacts above the active areas and buried bit lines between the cell contacts;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing dielectric material to form spacers within the buried bit line trenches and a dielectric layer within the cell contact trenches;

removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts while recessing the spacers within the buried bit lines; and

depositing conductive material within the buried bit line trenches and the cell contact trenches.

Claim 36 (currently amended): A method of forming electrical interconnects and buried bit lines in a semiconductor device comprising:

providing a substrate having two or more shallow-trench ~~insolated~~ insulated transistors with active areas therebetween and word lines traversing the active areas;

creating an insulating layer overlying the transistors, active areas and word lines;

patterning the insulating layer to define cell contacts above the active areas and buried bit lines above shallow trenches of the transistors;

removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches;

depositing dielectric material to form spacers within the buried bit line trenches and a dielectric layer within the cell contact trenches;

removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts while partially removing the spacers within the buried bit lines; and

depositing conductive material within the buried bit line trenches and the cell contact trenches.

Claim 37 (original): The method of claim 36, wherein the spacers comprise TEOS or silicon dioxide.

Claim 38 (original): A semiconductor device made according to the process of claim 34.

Claim 39 (original): A semiconductor device made according to the process of claim 35.

Claim 40 (original): A semiconductor device made according to the process of claim 36.

Claim 41 (new): The method of claim 34, wherein the spacers comprise TEOS or silicon dioxide.

Claim 42 (new): The method of claim 34, wherein the hard mask comprises polycrystalline silicon.

Claim 43 (new): The method of claim 42, wherein the hard mask has a thickness from about 1000 angstroms to about 2000 angstroms.

Claim 44 (new): The method of claim 34, wherein the hard mask comprises a tungsten compound.

Claim 45 (new): The method of claim 44, wherein the hard mask has a thickness from about 500 angstroms to about 1000 angstroms.

Claim 46 (new): The method of claim 35, wherein the spacers comprise TEOS or silicon dioxide.

Claim 47 (new): The method of claim 35, wherein the hard mask comprises polycrystalline silicon.

Claim 48 (new): The method of claim 47, wherein the hard mask has a thickness from about 1000 angstroms to about 2000 angstroms.

Claim 49 (new): The method of claim 35, wherein the hard mask comprises a tungsten compound.

Claim 50 (new): The method of claim 49, wherein the hard mask has a thickness from about 500 angstroms to about 1000 angstroms.

Claim 51 (new): The method of claim 36, wherein the hard mask comprises polycrystalline silicon.

Claim 52 (new): The method of claim 51, wherein the hard mask has a thickness from about 1000 angstroms to about 2000 angstroms.

Claim 53 (new): The method of claim 36, wherein the hard mask comprises a tungsten compound.

Claim 54 (new): The method of claim 53, wherein the hard mask has a thickness from about 500 angstroms to about 1000 angstroms.